Name:
Time:

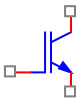
Lab 3: Power Switching Devices and Gating Circuits

Pre Lab

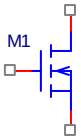
Be sure and bring your jumpers and breadboard to lab this week.

Power switching devices: While some engineers use transistors for their amplification properties, we power engineers use them for a much better purpose: switching.

1. Mark the names of the terminals of the IGBT below.



2. Mark the names of the terminals of the MOSFET below.

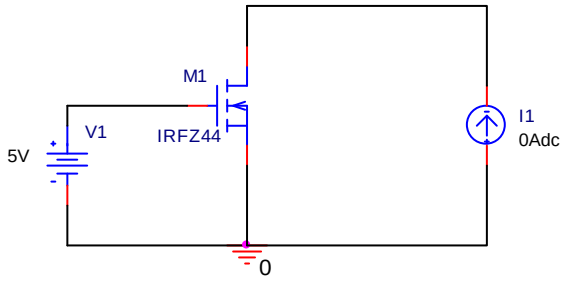


When an IGBT or BJT being used as a switch is "on," that means it's operating in the saturation region of its output curves. If it's somewhere in between we say it's in the active region and it's acting as an amplifier. When a MOSFET is being used as a switch, it's on in the triode region and off in the cutoff region. To avoid confusion from the different terms, we'll just refer to transistors as either on, active, or off. In order to be on, an IGBT must have enough voltage applied between its gate and emitter (V_{GE}) to be able to pass whatever collector current (I_C) is required by the circuit. Otherwise a large collector-emitter voltage (V_{CE}) develops and the transistor no longer behaves like a "good" switch. Substitute the words, "source" for emitter, and "drain" for collector and the same holds for a MOSFET.

3. Obtain a copy of the IRFZ44 datasheet.
4. Mark the on, active, and off regions of the output curves on the datasheet.

Consider the following theoretical circuit:

Name:
Time:



5. Using the curves, predict how large I1 can be before a large amount of voltage is dropped across the device, i.e before the device goes into the active region. Assume the junction temperature is 25^{o} C.

6. If an IRFZ44 has V_{GS}=7V and I_D=20A, what is V_{CE}?

In a perfect world a MOSFET or IGBT would go from "on" to "off" instantaneously. Of course that's not the case, though. It takes some time to switch between the different operating regions.

When a MOSFET or IGBT turns from off to on there are two time values that are important: turn-on delay ($t_{d,on}$) and rise time (t_r). Both can be found on the device's datasheet. The turn on delay is the amount of time it takes to charge the gate capacitance (more on gate capacitance later). The rise time is the time it takes for the device to turn fully on once the gate capacitance is charged. Both can be found on the device's datasheet.

7. What are typical $t_{d,on}$ and t_r values for the IRFZ44?

When a MOSFET or IGBT goes from on to off, there are two different time values to consider. Those are the turn off delay ($t_{d,off}$), and the fall time (t_f). The turn off delay is the time it takes to discharge the gate capacitance and the fall time is the time it takes for the device to turn off once the gate capacitance is discharged.

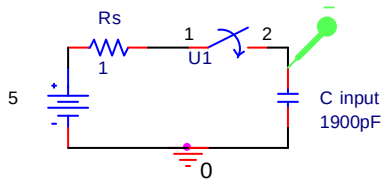
8. What are typical $t_{d,off}$ and t_f values for the IRFZ44?

9. Why do we care about switching times for power switching devices?

Name:
Time:

Gating Circuits

Mention was made above about the gate capacitance of a MOSFET or IGBT. Note: we'll restrict our discussion to MOSFETs, but IGBTs have similar gate characteristics. It's usually a valid assumption that the gate of a MOSFET looks like a pure capacitance for the first stage of turn on, then a large impedance for the rest of it. In order to turn the device on, that "gate capacitor" must be charged, and then the appropriate V_{GE} must be applied. To turn the device off, that gate capacitor must be discharged, and then V_{GE} must go sufficiently low. Consider the following theoretical circuit:

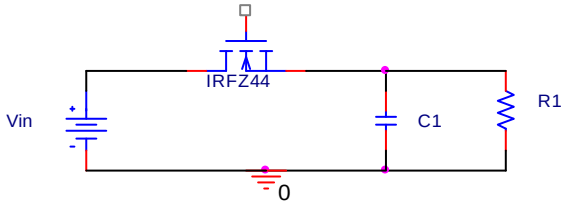


10. Do you expect the current into "C input" to be large or small right after the switch is closed?

11. If "C input" was the gate capacitance of a FET, and the designer tried to turn the FET off by opening the switch (removing the gate voltage), would the device every turn off? Why or why not?

Besides the problem of gate capacitance, there's another issue with gating power transistors you'll be looking at in lab today.

12. See if you can spot what that may be from looking at the following chopper circuit.



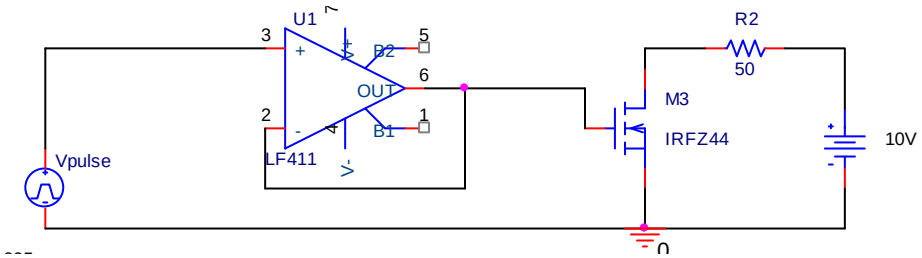
Lab Exercises

Gating Circuits:

We will often use opamps in this class to generate different gating signals. Let's see what happens when we try to gate a power transistor with an opamp.

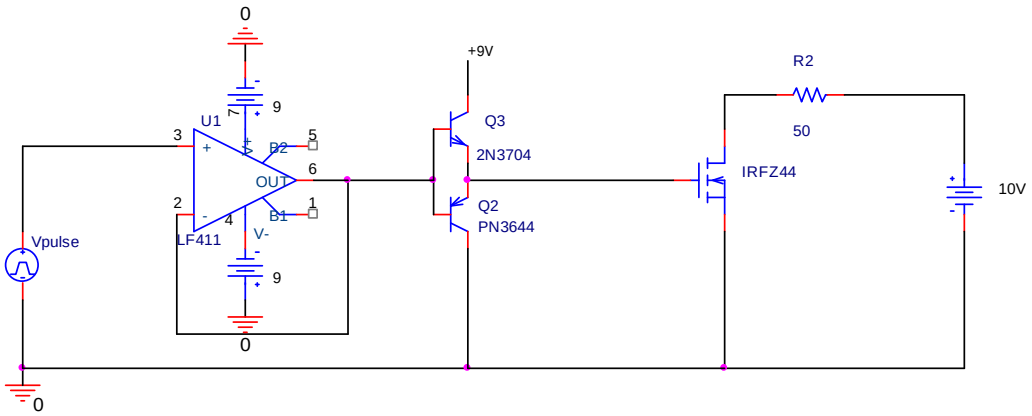
Name:
Time:

1. Build the following circuit on your breadboard. Use the function generator as Vpulse (0-5V pulses, 1 kHz). Use a power resistor for R2.



2. Run the circuit while measuring V_{DS} as well as V_{GE}. Use the LVDAC scope as well as the HP scope on the bench to watch those voltages.
3. Is the circuit working properly? Explain

4. Now put a totem pole (push-pull) gate driver in the circuit as shown below. A totem pole is capable of sourcing and sinking the currents needed to charge and discharge the gate capacitance and turn the device on and off.



5. Using the same scope setup as for number 3, draw a conclusion as to which circuit is better. Provide justification for your conclusion.

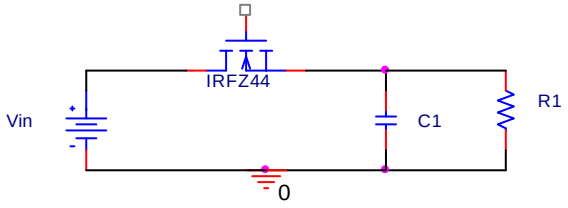
Name:
Time:

6. Predict what the V_{GS} pulses would look like if the input square wave pulses were changed to 0-3.3V.

7. Change the input square wave to 0-3.3V pulses and see if your prediction was correct. Does the totem pole gate driver provide any level shifting?

8. You would probably have drawn different conclusions if you had been using the LVDAC scope only. What conclusions can you draw about that instrument? In what situations is it ok to rely on the LVDAC scope and when should you use the HP scope?

The circuit you've been working with was nice in the fact that the source of the FET was on the ground. Therefore it was easy to get the correct voltage to the gate because we were able to reference everything to the same potential. What if we had been working with a circuit such as the one at the end of the pre lab?

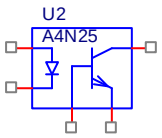


9. Assume that V_{in}=25V, and C1 is large enough that its voltage doesn't change very quickly (it's basically constant). If the voltage across C1 is 12.5V, what voltage with respect to ground needs to be applied to the gate of the FET if V_{GS} is to be 5V?

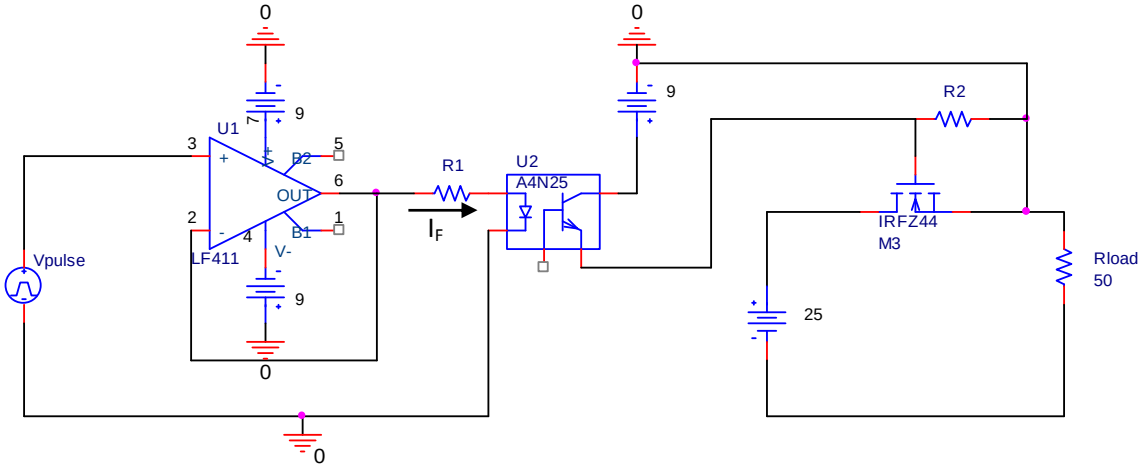
You can see how this problem could get out of control quickly in even a low voltage application. The way around this problem is to no longer reference everything to ground. Now we want to apply a voltage only between the gate and source of the FET. In other words, we want a control circuit with its ground at the source of the FET, and a power circuit that's referenced to some other potential. There are a

Name:
Time:

number of ways to do that; one common way is with an optocoupler or optoisolator. The symbol for the type of optocoupler we'll be using is this:



When the LED inside the optocoupler is lit it makes base current flow in the phototransistor, turning it on. You may come across optocouplers that don't have the base terminal of the phototransistor brought out of the case. That's because it's not essential to have it available. The base current will flow regardless of what's connected to the base, so it can be left open-circuited if you so choose. Here's how an optocoupler could fit into our chopper circuit:



The left-hand part of this circuit is the same function generator and buffer we used in the last part. Now if we have gate pulses of 5 V with respect to ground, the FET will turn on and we'll get 25 V across R_{load}. The optocoupler has allowed us to isolate the two parts of the circuit.

That's what an optocoupler does for us, so how do we go about choosing R1 and R2 to make it work? Here's a simple procedure:

a. Pick some mid-range value for R2, something like 10kΩ.
b. Calculate what the current that will flow through R2 when the phototransistor is on. Assume no current flows into the gate of M3.
c. Look at the $I_C - V_{CE}$ curves of the optocoupler on its datasheet. Find what I_F needs to be in order to ensure that the least amount of voltage possible is dropped across the phototransistor. I.e find what I_F needs to be to saturate the phototransistor.

Name:
Time:

d. Calculate what R1 needs to be to make that current flow through the LED. Be sure to take into account the forward voltage drop across the LED, which can be found on the datasheet.

10. Build the circuit and choose R1 and R2 so that it works. Include a screenshot of V_{GS} and the voltage across R_{load} from the LVDAC scope. What did you choose for R1 and R2?

Power Switching devices:

1. Set up a buck chopper on the Lab Volt Chopper/Inverter module. Use 20Vdc as the input and put a 150 Ω load on the output. Run the chopper at 60% duty cycle and 1kHz.
2. Use the LVDAC scope to watch the gating signal (from the Q1 switching control terminal to the white switching control ground terminal). Also watch the voltage across Q1.
3. Using a screenshot of the scope and some explanation, show which modes the IGBT operates in for this circuit.

Name:
Time:

4. The IGBTs in the IGBT Chopper/Inverter are IRG4PC30KD's. What is the rated turn-on delay and rise time for that IGBT?

5. Use the HP scope to view the gating signal and estimate the turn-on delay, rise time, turn-off delay, and fall time for the IGBT in the buck chopper circuit.

6. Estimate the average power loss from switching as well as the overall average power loss. To do this you should look at the voltage across the IGBT and the current through it on the LVDAC scope. Use screenshots to justify your answers.